

WHAT IS CLAIMED IS:

- 1 1. A process for depositing a film on a substrate disposed in a
2 processing chamber, said process comprising the steps of:
3 (a) introducing a process gas into said process chamber;
4 (b) applying RF power to an inductively coupled coil to form
5 a plasma from said process gas and deposit a first layer of said film over said
6 substrate during a first time period;
7 (c) maintaining said plasma during a second time period
8 subsequent to said first time period and biasing said plasma toward said substrate to
9 promote a sputtering effect of said plasma and deposit a second layer of said film over
10 said first layer.
- 1 2. The process of claim 1 wherein said biasing step is performed
2 by applying RF power to capacitively coupled electrodes.
- 1 3. The process of claim 1 wherein said second time period is at
2 least 10 times longer than said first time period.
- 1 4. The process of claim 1 wherein said process gas comprises
2 silicon and oxygen and said deposited film is a silicon oxide film.
- 1 5. The process of claim 4, wherein said silicon oxide film is
2 deposited at a temperature of between about 200-425 °C.
- 1 6. The process of claim 4, wherein said silicon oxide film is
2 deposited at a pressure of between about 1-25 millitorr.
- 1 7. The process of claim 4, wherein said silicon oxide film is
2 deposited at a temperature of between about 375-400°C and at a pressure of between
3 about 4-7 millitorr.

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1 8. The process of claim 2, wherein the application of RF power to
2 said capacitively coupled electrodes is delayed between about 1 to 100 seconds while
3 the application of RF power to said inductively coupled coil is maintained.

1 9. The process of claim 8, wherein the application of RF power to
2 said capacitively coupled electrodes is delayed between about 5 to 20 seconds while
3 the application of RF power to said inductively coupled coil is maintained.

1 10. The process of claim 1, wherein said first layer is deposited to a
2 thickness of between about 1 to 15 percent of the thickness to which said second layer
3 is deposited.

1 11. The process of claim 1, wherein said film is about 1.0 microns
2 or less and said first layer is about 0.15 microns or less thick.

1 12. The process of claim 1 wherein said process gas comprises
2 silane and oxygen.

1 13. The process of claim 12 wherein said process gas further
2 comprises argon.

1 14. In a high-density plasma chemical vapor deposition chamber
2 having an inductively coupled coil and capacitively coupled electrodes, a process for
3 depositing a film on a substrate, said process comprising the steps of:

- 4 (a) introducing a process gas into said chamber;
5 (b) applying RF power to said inductively coupled coil to
6 form a plasma from said process gas and deposit a first layer of said film over said
7 substrate;
8 (c) maintaining said inductively coupled plasma and applying
9 RF power to said capacitively coupled electrodes to bias said plasma toward said
10 substrate, thereby promoting a sputtering effect of said plasma and depositing a
11 second layer of said film.

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- 1 15. The process of claim 14 further comprising the steps of:
 2 (d) maintaining said inductively coupled plasma and
 3 removing RF power from said capacitively coupled electrodes to stop biasing said
 4 plasma toward said substrate and deposit a third layer of said film over said substrate;
 5 (e) maintaining said inductively coupled plasma and applying
 6 RF power to said capacitively coupled electrodes to bias said plasma toward said
 7 substrate, thereby promoting a sputtering effect of said plasma and depositing a fourth
 8 layer of said film;
 9 (f) repeating steps (d) and (e) iteratively until a selected
 10 thickness of said film is reached.

1 16. An integrated circuit formed on a semiconductor substrate by the
 2 method of claims 1, 14 or 15.

- 3 17. A high-density plasma chemical vapor deposition system
 4 comprising:
 5 a housing for forming a vacuum chamber;
 6 a vacuum pump for evacuating said vacuum chamber;
 7 a pedestal, located within said housing, for holding a semiconductor
 8 substrate;
 9 a gas distribution system for introducing a process gas into said vacuum
 10 chamber;
 11 a plasma generation system for creating an inductively coupled plasma
 12 from said process gas within said vacuum chamber and for biasing said plasma toward
 13 said substrate to enhance sputtering;
 14 a controller for controlling said vacuum pump, said gas distribution
 15 system and said plasma generation system;
 16 a memory coupled to said controller and storing a program for
 17 directing the operation of said system, said program including a set of instructions for
 18 depositing a stress-reduced film by
 first, controlling said gas distribution system to introduce said
 process gas into said chamber;

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19 second, controlling said plasma generation system to apply RF
20 power to said inductively coupled coil to form a plasma from said process gas and
21 deposit a first layer of said film over said substrate; and

22 third, controlling said plasma generation system to maintain said
23 inductively coupled plasma and bias said plasma toward said substrate, thereby
24 promoting a sputtering effect of said plasma and depositing a second layer of said
25 film.

1 18. The apparatus of claim 17 wherein said program further includes
2 instructions for depositing a plurality of said first layers and said second layers by

3 fourth, controlling said plasma generation system to maintain
4 said inductively coupled plasma and stop biasing said plasma toward said substrate;

5 fifth, controlling said plasma generation system to maintain said
6 inductively coupled plasma and bias said plasma toward said substrate, thereby
7 promoting a sputtering effect of said plasma; and

8 sixth, performing the second and third steps iteratively at least
9 once until a desired thickness of said film is reached.

1 19. The apparatus of claim 17 wherein said gas distribution system
2 is adapted to introduce a process gas comprising silicon and oxygen into said
3 chamber.

1 20. A high-density plasma chemical vapor deposition system
2 comprising:

3 a housing for forming a vacuum chamber;

4 a pedestal, located within said housing, for holding a semiconductor
5 substrate;

6 means for introducing reactants into said vacuum chamber, said
7 reactants including silicon and oxygen;

8 means for generating an inductively coupled plasma from said reactants
9 to deposit a first layer of a silicon oxide film on said semiconductor substrate during a
10 first time period, said first layer for the reduction of mechanical stress in a
11 subsequently deposited layer of a silicon oxide film; and

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12 means for biasing said plasma toward said substrate during a second
13 time period after said first time period to enhance a sputtering of said plasma and
14 deposit said subsequent layer.

1 21. The apparatus of claim 20, further comprising means for
2 maintaining a pressure of between about 0.001-10 torr in said vacuum chamber while
3 said films are deposited.

1 22. The apparatus of claim 20, further comprising means for
2 maintaining a wafer temperature of between about 100-500 °C in said vacuum
3 chamber while said films are deposited.

1 23. An integrated circuit formed on a semiconductor substrate, said
2 integrated circuit comprising:

3 (a) a plurality of active devices formed in said semiconductor
4 substrate;

5 (b) at least one metal layer formed above said semiconductor
6 substrate; and

7 (c) at least one insulating layer formed between said metal layer and
8 said semiconductor substrate, said insulating layer having a plurality of patterned
9 holes filled with electrically conductive material to electrically connect selected
10 portions of said metal layer to selected portions of said semiconductor substrate,
11 wherein said insulating layer comprises a first silicon oxide layer and a second silicon
12 oxide layer, said first and said second silicon oxide layers deposited using a high-
13 density plasma chemical vapor deposition process, said first silicon oxide layer
14 deposited for the reduction of mechanical stress in said second silicon oxide layer.

1 24. The integrated circuit of claim 23, further comprising:

2 (d) a second metal layer formed above said semiconductor substrate
3 and below said at least one insulating layer;

4 (e) a second insulating layer formed between said second metal
5 layer and said semiconductor substrate, said second insulating layer having a second
6 plurality of patterned holes filled with electrically conductive material to electrically

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- 7 connect selected portions of said second metal layer to selected areas of said plurality
8 of active devices.

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